Figure 1

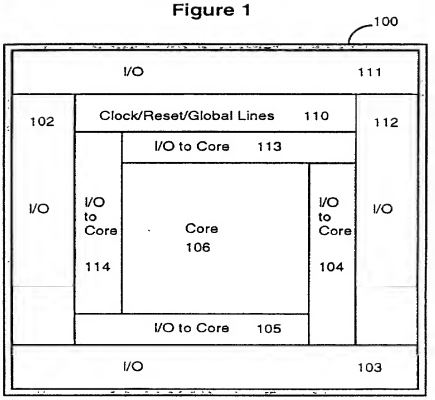

100
I/O
111
102
Clock/Reset/Global Lines
110
112
I/O to Core
113
I/O
I/O to Core
114
Core
106
I/O to Core
104
I/O
I/O to Core
105
I/O
103

Figure 2A

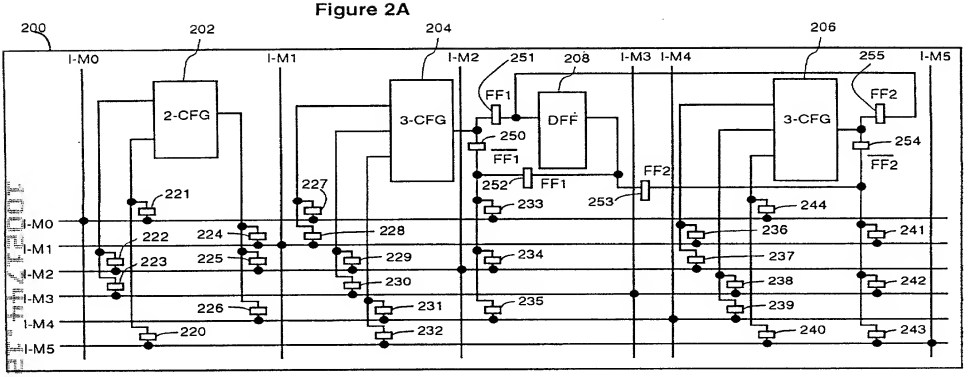


Figure 2B

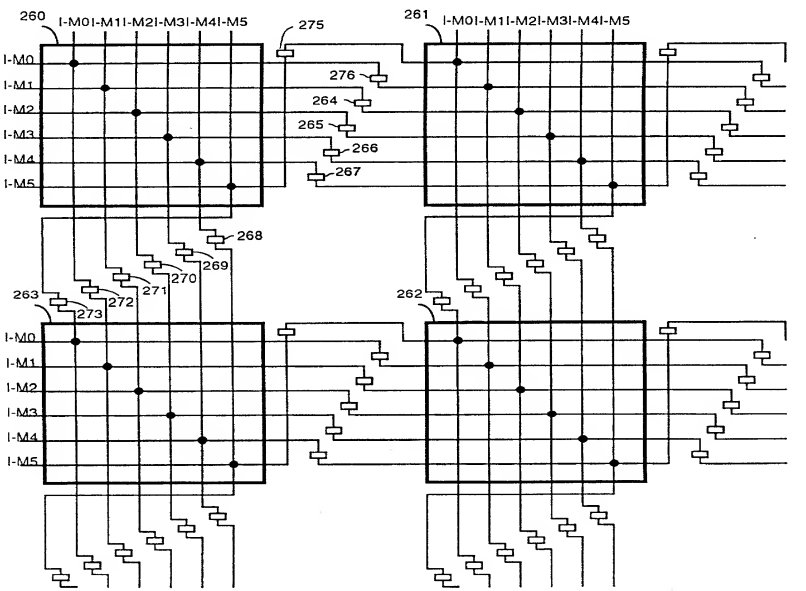


Figure 3A

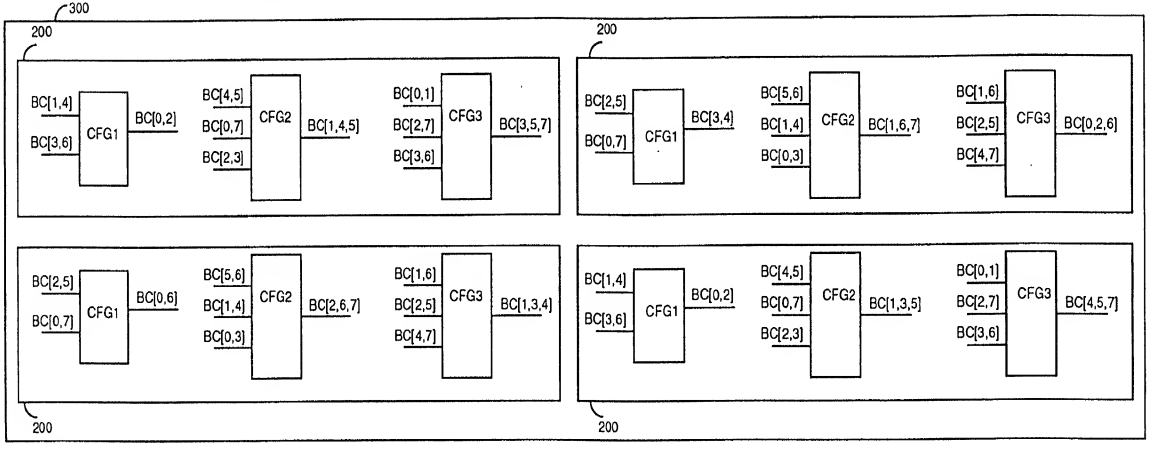
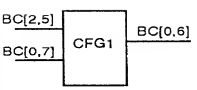

300
200
BC[1,4]
BC[3,6]
CFG1
BC[0,2]
BC[4,5]
BC[0,7]
BC[2,3]
CFG2
BC[1,4,5]
BC[0,1]
BC[2,7]
BC[3,6]
CFG3
BC[3,5,7]
200
BC[2,5]
BC[0,7]
CFG1
BC[3,4]
BC[5,6]
BC[1,4]
BC[0,3]
CFG2
BC[1,6,7]
BC[1,6]
BC[2,5]
BC[4,7]
CFG3
BC[0,2,6]
BC[2,5]
BC[0,7]
CFG1
BC[0,6]
BC[5,6]
BC[1,4]
BC[0,3]
CFG2
BC[2,6,7]
BC[1,6]
BC[2,5]
BC[4,7]
CFG3
BC[1,3,4]
200
BC[1,4]
BC[3,6]
CFG1
BC[0,2]
BC[4,5]
BC[0,7]
BC[2,3]
CFG2
BC[1,3,5]
BC[0,1]
BC[2,7]
BC[3,6]
CFG3
BC[4,5,7]
200

Figure 3B



EQUALS

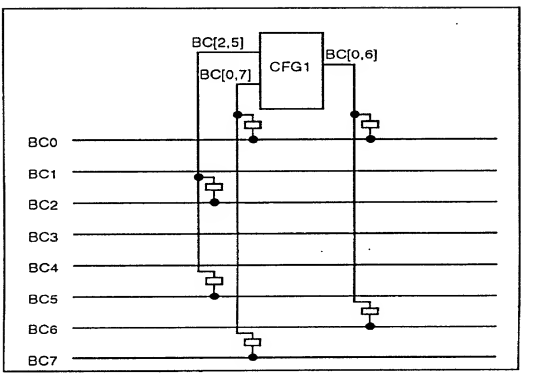
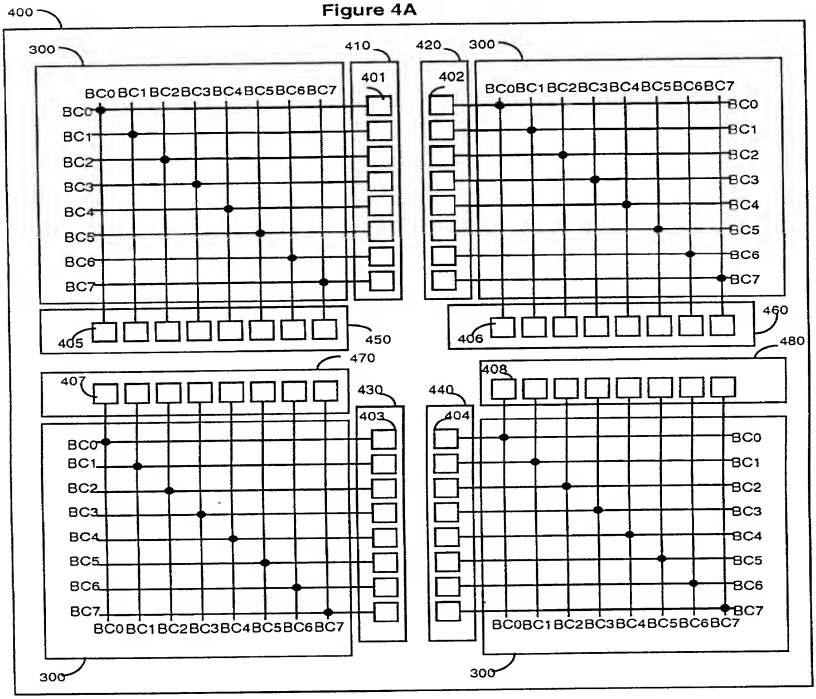


Figure 4A



: BC Tab Network

Figure 4B

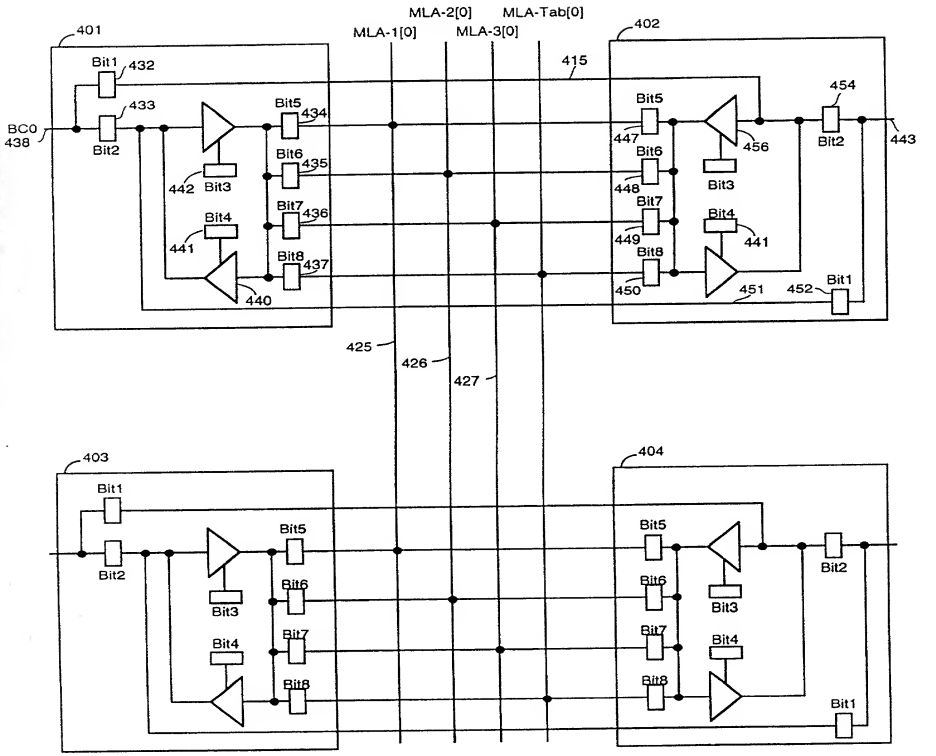

MLA-2[0]
MLA-Tab[0]
MLA-1[0]
MLA-3[0]
401
402
403
404
415
425
426
427
BC0
438
Bit1
Bit2
Bit3
Bit4
Bit5
Bit6
Bit7
Bit8
432
433
434
435
436
437
440
441
442
443
447
448
449
450
451
452
454
456

Figure 4C

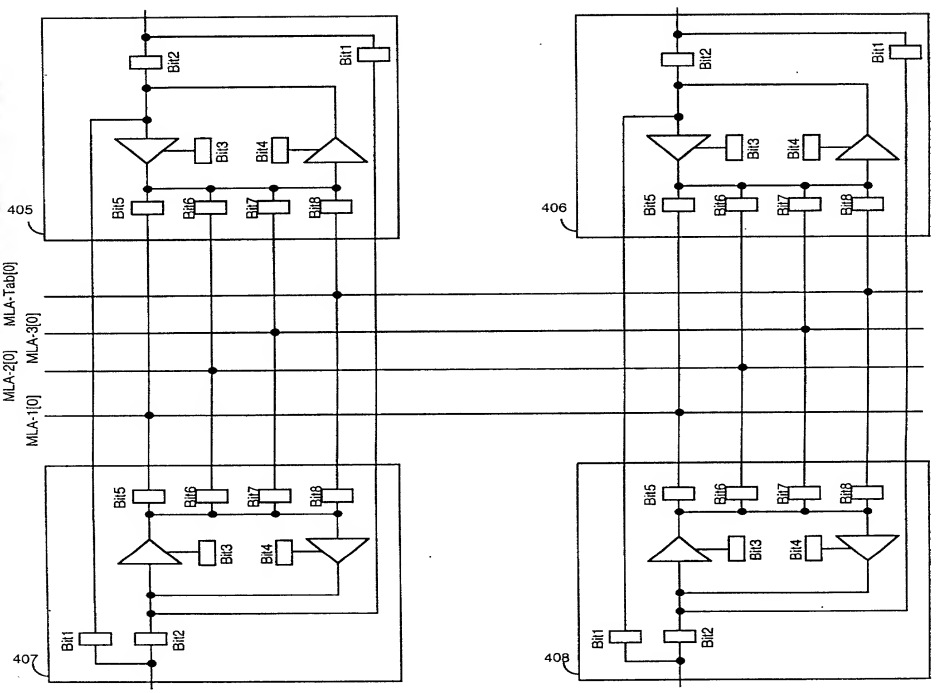

405
406
407
408
Bit1
Bit2
Bit3
Bit4
Bit5
Bit6
Bit7
Bit8
MLA-2[0]
MLA-1[0]
MLA-Tab[0]
MLA-3[0]

Figure 5

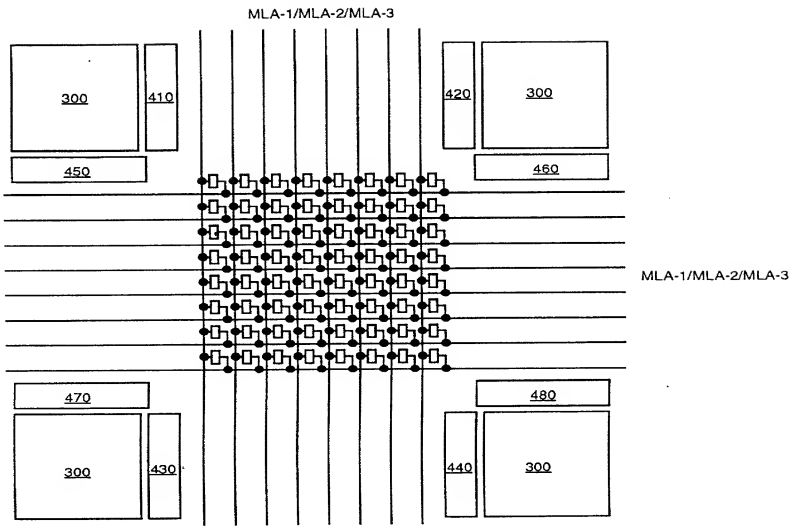
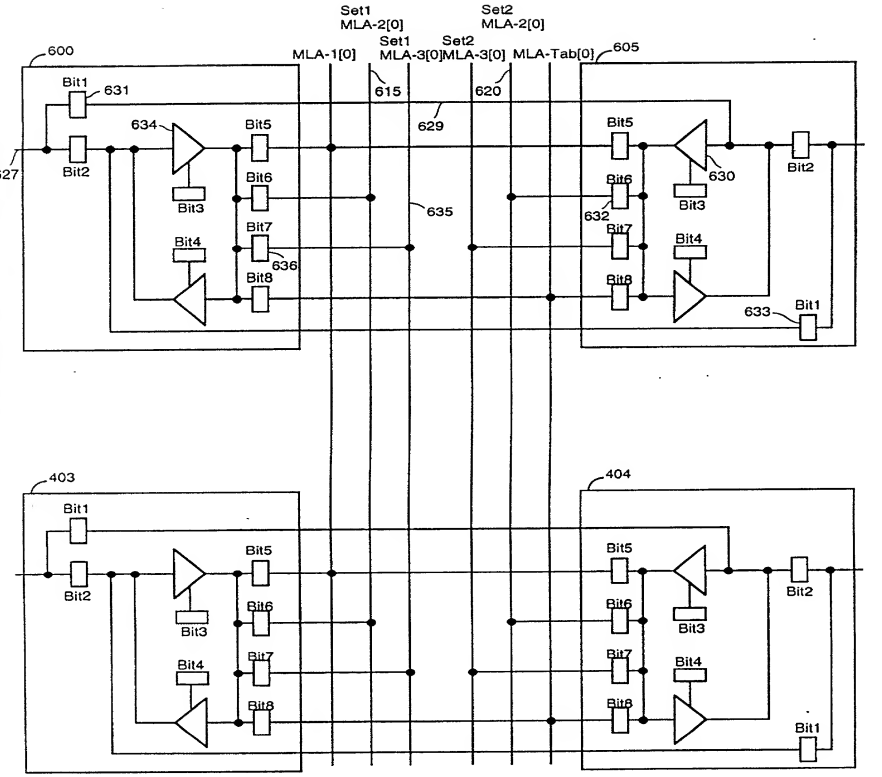

MLA-1/MLA-2/MLA-3
300
410
420
300
450
460
MLA-1/MLA-2/MLA-3
470
480
300
430
440
300

Figure 6A


Set1
MLA-2[0]
Set2
MLA-2[0]
Set1
MLA-3[0]
Set2
MLA-3[0]
MLA-1[0]
MLA-Tab[0]
600
605
615
620
629
627
631
634
635
630
632
633
636
Bit1
Bit2
Bit3
Bit4
Bit5
Bit6
Bit7
Bit8
403
404

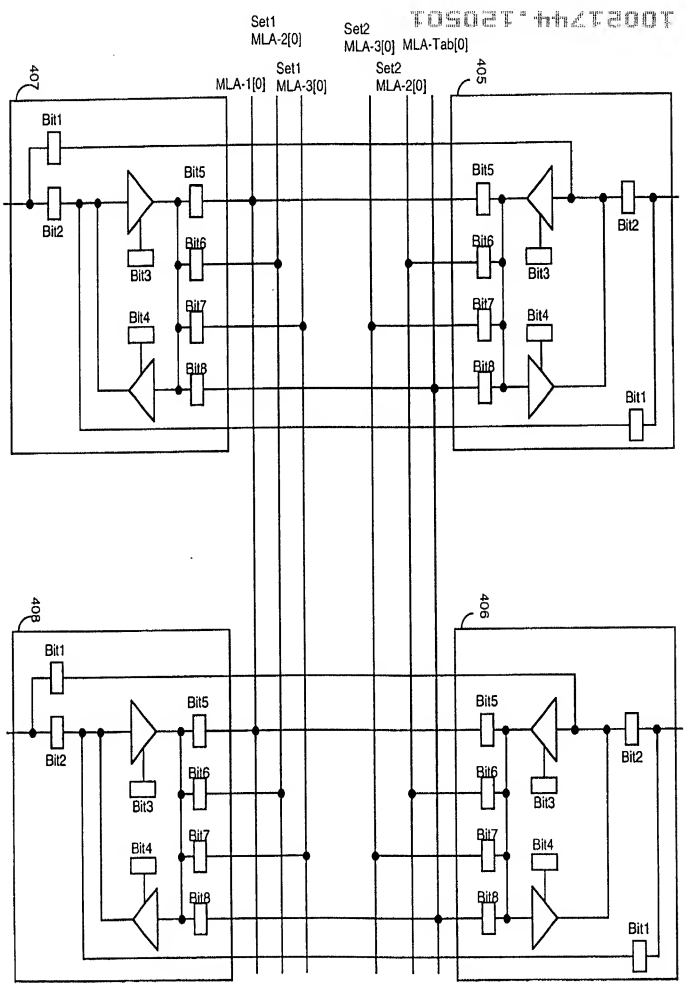

Set1
MLA-2[0]
Set2
MLA-3[0]
MLA-Tab[0]
Set1
MLA-3[0]
Set2
MLA-2[0]
MLA-1[0]
407
405
408
406
Bit1
Bit2
Bit3
Bit4
Bit5
Bit6
Bit7
Bit8

Figure 6B

Figure 7A

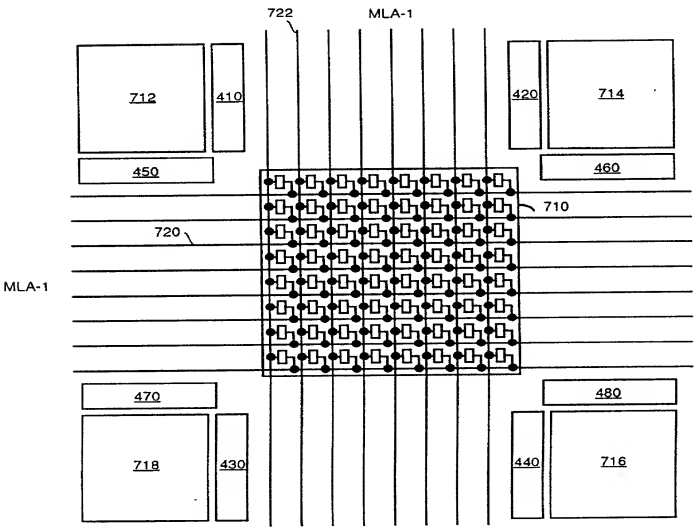

722
MLA-1
712
410
420
714
450
460
710
720
MLA-1
470
480
718
430
440
716

Figure 7B

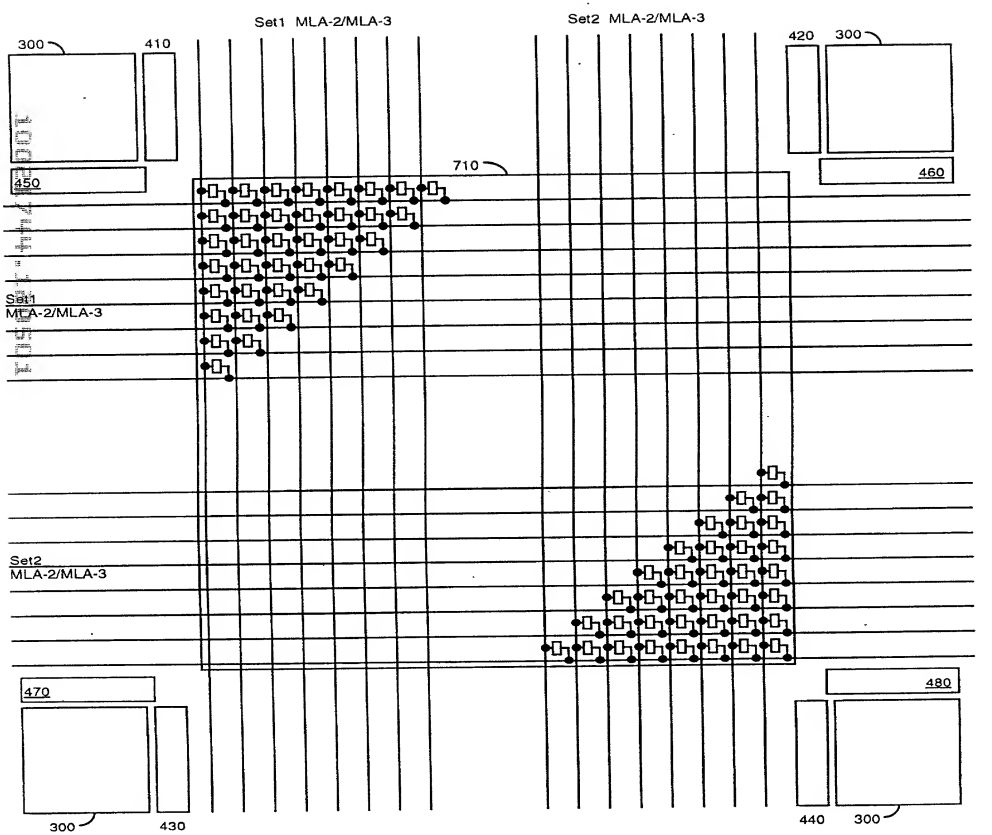

Set1 MLA-2/MLA-3
Set2 MLA-2/MLA-3
300
410
420
300
710
450
460
Set1
MLA-2/MLA-3
Set2
MLA-2/MLA-3
470
480
300
430
440
300

Figure 7C

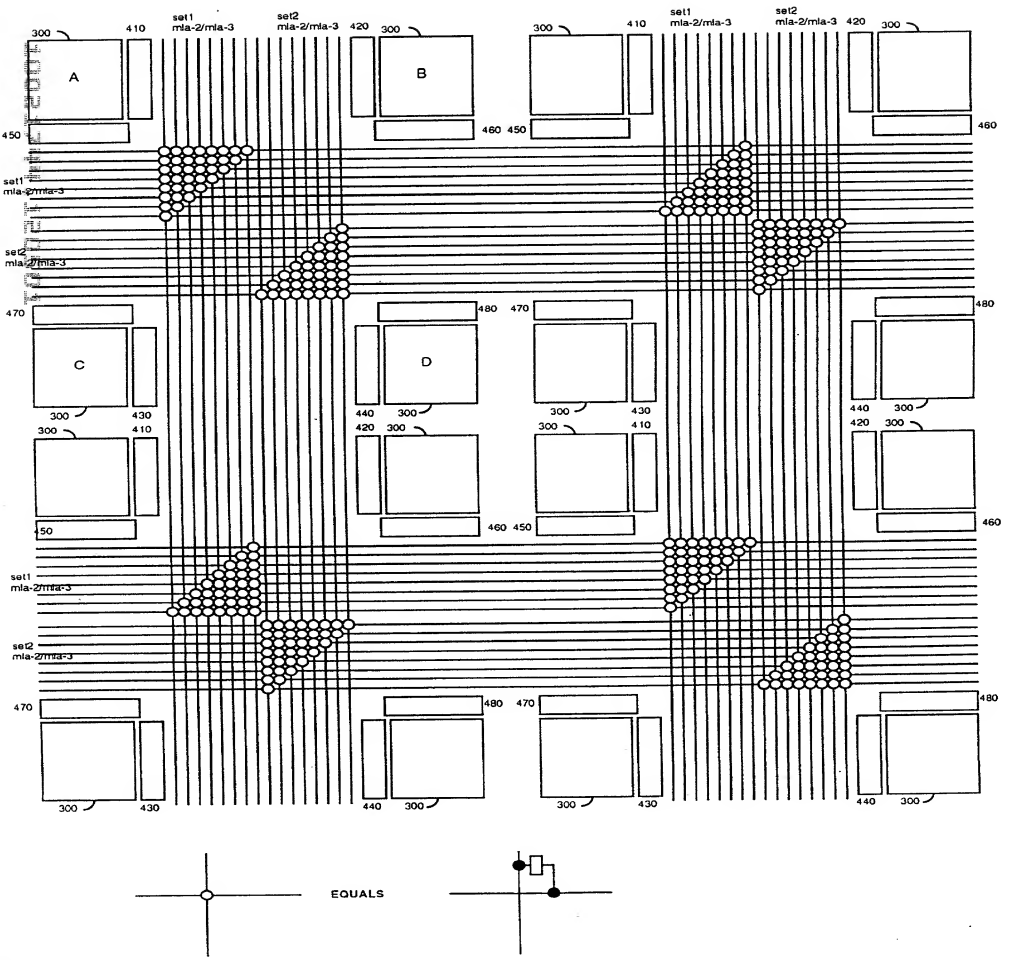

A
B
C
D
300
410
420
430
440
450
460
470
480
set1
mla-2/mla-3
set2
mla-2/mla-3
EQUALS

Figure 8A: Layout Floor Plan for a Logic Block

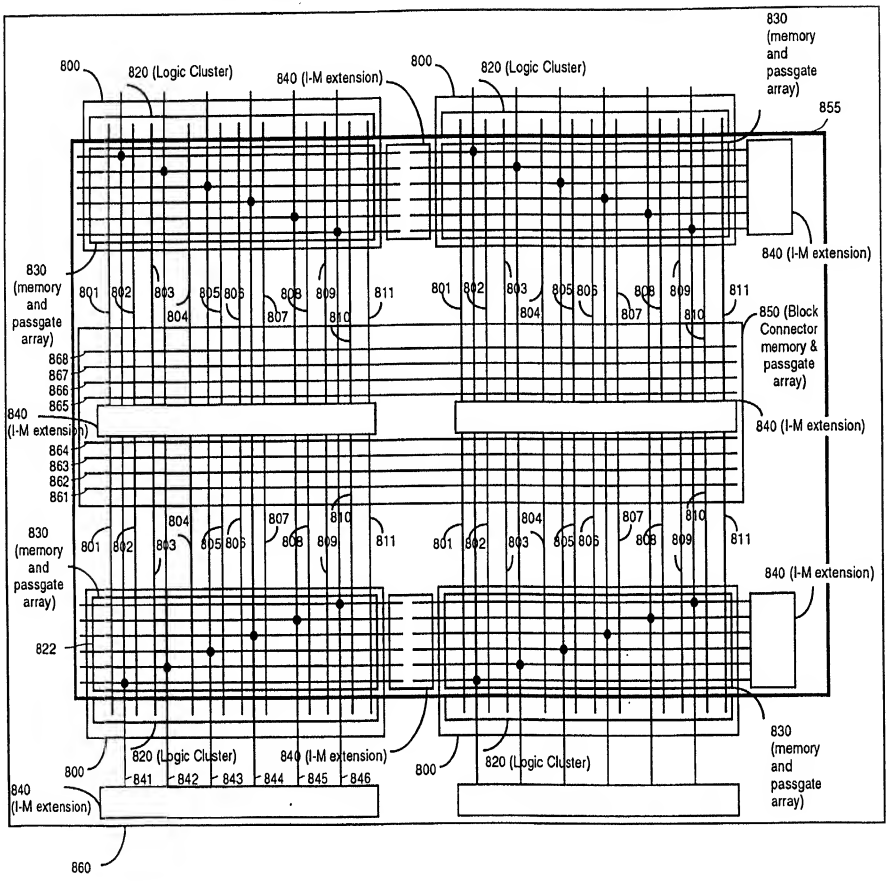


Figure 8B: Layout Floor Plan for a 2x2 Logic Block with Associated MLAs

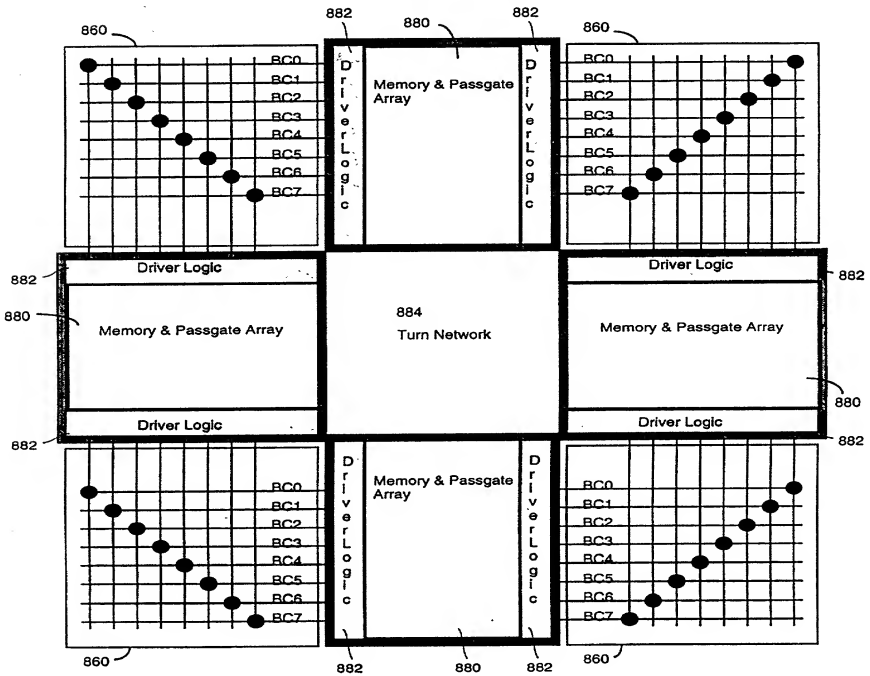
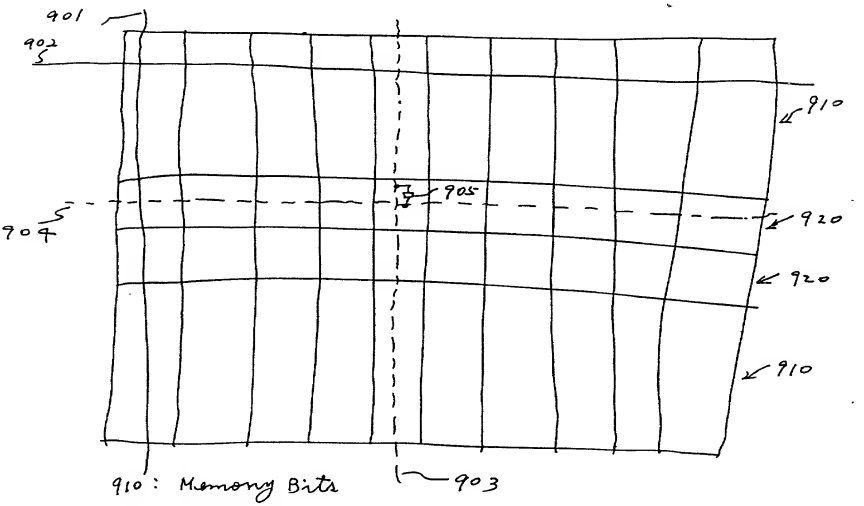


Figure 9 Example of Contiguous Memory and passgate Array Layout Organization



910 : Memory Bits

920 : Passgates

901, 902 : addressing lines X-Y

903, 904 : Routing Lines

905 : Program controlled passgate between 903 and 904